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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/620,284	07/14/2003	Robert C. Pack	CA7010502001	7731

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EXAMINER	
TAT, BINH C	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 04/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H·A

Office Action Summary	Application No.	Applicant(s)	
	10/620,284	PACK ET AL.	
	Examiner	Art Unit	
	Binh C. Tat	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-44* is/are pending in the application.

4a) Of the above claim(s) *15-22 and 37-44* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14 and 23-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07/14/05* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 08/24/04, 06/25/04, 10/31/03
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/620284 filed on 06/24/03.

Claims 1-44 remain pending in the application.

Election/Restrictions

Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-14, 23-36 drawn to design mask, classified in class 716, subclass 19+, interfeature relationships of the integrated circuit.

II. Claims 15-27 drawn to mask inspection, classified in class 716, subclasss 19+, design data comprise polygonal shape.

III. Claims 37-44 drawn to mask inspection, classified in class 716, subclasss 19+, design data comprise polygonal shape.

During a telephone conversation with Peter C. Mei on 04/15/05 a provisional election was made without traverse to prosecute the invention of group I, claims 1-14, and 23-36. Applicant in replying to this Office action must make affirmation of this election. Claims 15-27, and 37-44 are canceled.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-14, and 23-36 are rejected under 35 U.S.C. 102(e) as being anticipated by Randallet al. (U.S Patent 6634018).

3. As to claims 1, and 23 Randallet al. teach a method for writing a mask, comprising: generating integrated circuit design data (see fig 7 col 7 lines 39-57); and using information for interfeature relationships of the integrated circuit design data to inspect the mask (see fig 7 and col 4 lines 17-46 and col 7 lines 58 to col 8 lines 67).

4. As to claim 2, and 24 Randallet al. teach wherein the interfeature relationships are on one layer of the integrated circuit design (see col 2 lines 10-24 and col 4 lines 25-61).

5. As to claim 3, and 25 Randallet al. teach wherein the interfeature relationships am across multiple layers of the integrated circuit design (see col 2 lines 10-24 and col 4 lines 25-61).

6. As to claim 4, and 26 Randallet al. teach wherein the interfeature relationships comprise: interfeature process proximity effects (see col 2 lines 26 to col 4 lines 4); interfeature coupling across layers (see col 2 lines 10-24 and col 4 lines 25-61); interfeature electronic relationships (see col 2 lines 26 to col 4 lines 4); or wire interconnects longer than a given length (see col 2 lines 26 to col 4 lines 4).

7. As to claim 5, and 27 Randallet al. teach wherein the information for interfeature relationships includes information for identifying a redundancy of features, and using the information for interfeature relationships to inspect the mask further comprises: determining that at least one feature is functional (see col 3 lines 57 to col 4 lines 16 and col 5 lines 14 to col 6 liens 19); and waiving one or more defects on features redundant to the functional feature (see col 3 lines 57 to col 4 lines 16 and col 5 lines 14 to col 6 liens 19).

8. As to claim 6, and 28 Randallet al. teach a method for generating a lithography mask or a printed wafer, comprising: generating integrated circuit design data (see fig 7 col 7 lines 39-57);

and using context information from the integrated circuit design data to inspect the photomask wafer (see fig 7 and col 4 lines 17-46 and col 7 lines 58 to col 8 lines 67).

9. As to claim 7, and 29 Randallet al. teach wherein using context information comprises: identifying to individual mask features or groups of mask features information relating to circuit elements intended to be produced from those mask features as defined in the integrated circuit design data (see col 6 lines 42 to col 7 lines 50).

10. As to claim 7, and 29 Randallet al. teach wherein using context information comprises: analyzing mask features for contextual priority (see col 2 lines 26 to col 4 lines 4).

11. As to claim 8, and 30 Randallet al. teach wherein using context information comprises: assigning priorities to the mask features (see col 2 lines 26 to col 4 lines 4).

12. As to claim 9, and 31 Randallet al. teach wherein assigning priorities to the mask features comprises: applying criteria to mask design data by manual process (see col 3 lines 57 to col 4 lines 16 and col 5 lines 14 to col 6 liens 19).

13. As to claim 10, and 32 Randallet al. teach wherein assigning priorities to the mask features comprises: applying criteria to mask design data by computer-aided automated process (see col 3 lines 57 to col 4 lines 16 and col 5 lines 14 to col 6 liens 19 and background).

14. As to claim 11, and 33 Randallet al. teach wherein using context information comprising: analyzing mask features to determine the circuit element expected to be produced by a lithography system at a chip wafer surface (see col 3 lines 57 to col 4 lines 16 and col 5 lines 14 to col 6 liens 19 and background).

15. As to claim 12, and 34 Randallet al. teach further comprising: configuring a mask design database to include additional contextual mask design data generated in using the contextual

information from the integrated circuit design data (see fig 7 and col 4 lines 17-46 and col 7 lines 58 to col 8 lines 67).

16. As to claim 13, and 35 Randallet al. teach further comprising: configuring the mask design database to optimize an order of mask design data for use by a mask inspection system.

17. As to claim 14, and 36 Randallet al. teach wherein using context information comprises: information for neighboring geometries, electrical intent of the features, timing of the intended circuit, redundant features, and relationships of a given feature to neighboring feature (see col 3 lines 57 to col 4 lines 16 and col 5 lines 14 to col 6 liens 19).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Binh C. Tat whose telephone number is (571) 272-1908. The examiner can normally be reached on 7:30 - 4:00 (M-F).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mathew Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Binh Tat
Art unit 2825
April 15, 2005

Thuando
THUAN DO
Primary examiner.
04/17/2005.